Modeling of Transverse Propagation Delays in the GaAs/AlGaAs Modulation Doped Heterojunction Field Effect Transistors

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Abstract—**We have developed a computer-efficient algorithm to calculate the transverse propagation delays in a GaAs/AlGaAs MODFET. The model includes the intrinsic as well as the extrinsic parameters of the MODFET. The dependences of these delays on the various MODFET parameters such as its gate length, width and the gate metal resistivity have been studied.**

I. Introduction

In the recent past, a numerical model of the transverse propagation delays in GaAs MESFETs was presented [1]. In this paper, the numerical technique has been extended to study the transverse delays in a GaAs/AlGaAs MODFET. A three-dimensional model has been set up to model the two lossy gate and drain lines coupled to each other via the gate-drain capacitances. Intrinsic as well as the extrinsic parameters are taken into account in this model. The algorithm has been used to analyze the dependences of these delays on the various MODFET parameters. Results can be utilized for the optimization of picosecond circuits.

II. The Model

A GaAs/AlGaAs MODFET modeled as two lossy transmission lines coupled to each other by the gate-drain distributed capacitances is shown in Fig. 1. As for the MESFET [1], the gate line was fed by a unit step voltage signal on one end while its other end was open circuited. The various symbols used in Fig. 1 and the following analysis are: ε = semiconductor permittivity; μ_0 = low-field carrier mobility; V_1 = effective voltage along the gate width; W = channel width or gate width; L_g = gate length; G_o = output conductance; R_{ss} = source resistance; R_{gg} = gate series resistance; R_{dd} = drain series resistance; C_o = gate charging capacitance per unit area; d_o = distance between two-dimensional electron gas and the gate electrode; v_{sat} = saturation velocity of electrons in the channel; C_{gd} = gate-to-drain feedback capacitance; C_{ds} = drain-to-source output capacitance; G_m = transconductance; L_{gg} = inductance of the gate line; L_{dd} = inductance of the drain line; Z_L = load impedance; V_s = unit step voltage; C_g = effective capacitance of the depletion layer under the gate; V_g = voltage across the capacitance C_g; and, R_i = effective intrinsic resistance between gate and source.

A. Drain Current

Following the same steps as for the MESFET [1], it can be shown that the current induced in one section of the drain line for a MODFET is given by

$$dI(s) = \frac{-G_1 G_5}{(G_1 + G_3 - G_5)} \cdot \frac{1}{\cosh(\gamma W)} \frac{\cosh[\gamma(W-z)]}{s}\, dz \tag{1}$$

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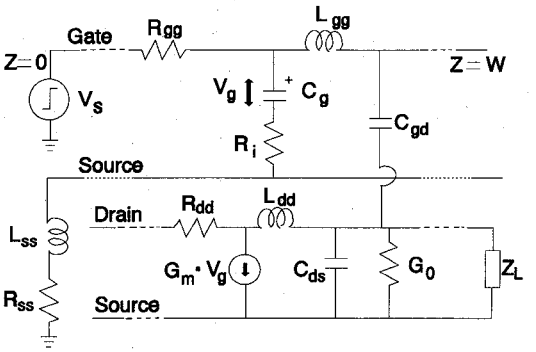

Fig. 1. A GaAs/AlGaAs MODFET modeled as two lossy transmission lines coupled to each other the distributed capacitance C_{gd}.

where dz is the length of the section along the width of the MODFET, γ is the propagation constant,

$$G_1 = \frac{sC_g}{1+sC_gR_i}; \qquad G_3 = \frac{1}{R_{ss}+sL_{ss}};$$
$$G_5 = \frac{\frac{G_mDG_3}{G_1} + \frac{G_2G_3}{G_1}}{\frac{G_mD}{G_1} + \frac{G_2}{G_c} + \frac{G_2}{G_1} + 1}; \qquad D = \frac{1}{1+sR_iC_g};$$
$$G_2 = G_o + sC_{ds}; \quad \text{and} \quad G_c = sC_{gd}. \tag{2}$$

The total current induced in the drain line will then be given by

$$I(s) = \frac{-G_1G_5}{\cosh(\gamma W)s(G_1+G_3-G_5)} \cdot \int_0^W \cosh[\gamma(W-z)]\, dz \tag{3}$$

The output drain current $i(t)$ in the time domain was then obtained by an inverse Laplace transformation of $I(s)$.

B. MODFET Parameters

Instead of using the various values of parameters published in the literature, the following physical equations were used to determine the values of the MODFET parameters used in Fig. 1. The transconductance G_m is given by [2], [3]:

$$G_m = \beta_1 V_c(1-\gamma_1)\frac{e^{\left(\frac{-j\omega k_0\tau_0}{a}\right)}}{1+\frac{j\omega\tau_0}{a}} \tag{4}$$

$$\beta_1 = \frac{WC_o\mu_o}{L_g}; \qquad V_c = \frac{L_g\nu_{\text{sat}}}{\mu_o}; \qquad \gamma_1 = \frac{1}{\sqrt{\left(1+\frac{2V_1}{V_c}\right)}};$$
$$\tau_o = \frac{2\gamma_1 L_g}{3\nu_{\text{sat}}(1-\gamma_1)}; \qquad k_o = 0.61; \qquad a = 39. \tag{5}$$

and ω is the imaginary value of s in the s-plane. The capacitance C_g was calculated by using the (2) and (3):

$$C_g = C_{g1} + C_{g2}; \qquad C_{g1} = \frac{2}{3}\gamma_1 C_o W L_g;$$
$$C_{g2} = (1-\gamma_1)W(L_g+\Delta L_g)C_o \tag{6}$$

ΔL_g is the additional effective gate length because the depletion layer under the gate electrode extends beyond the actual gate length. The resistance R_i is given by [2], [3]:

$$R_i = \frac{R_{i1}}{\left[1+\frac{C_{g2}}{C_{g1}}\right]}; \qquad R_{i1} = \frac{1}{5\beta_1 V_c(1-\gamma_1)} \tag{7}$$

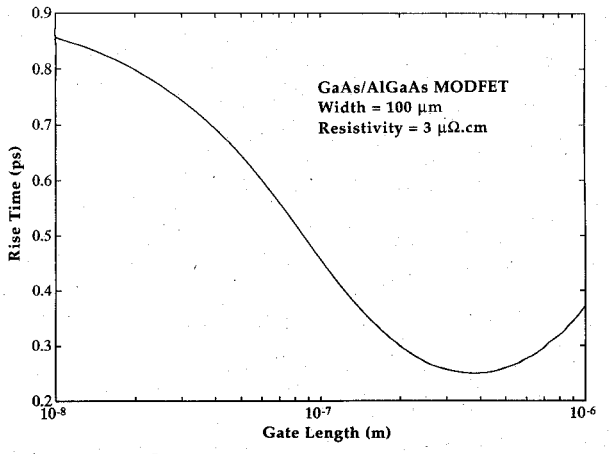

Fig. 2. Dependence of the rise time on the gate length in a typical GaAs/AlGaAs MODFET in the range $0.01-1$ μm.

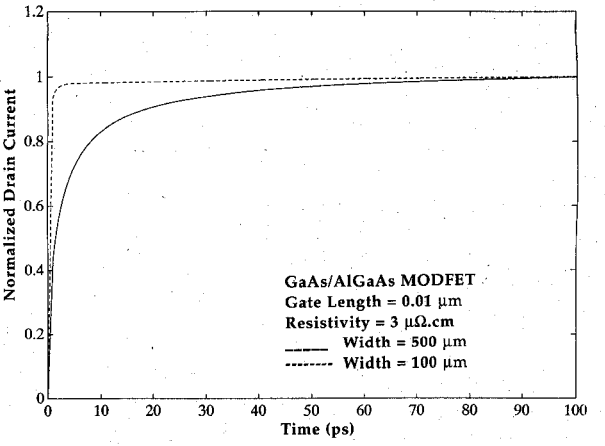

Fig. 3. Normalized short-circuited drain currents in a GaAs/AlGaAs MODFET for the widths of 100 and 500 μm in the time range 0–100 ps.

The capacitances C_{gd} and C_{ds} were calculated by using the expressions [2], [3]:

$$C_{gd} = W\varepsilon; \qquad C_{ds} = W\varepsilon\frac{K(m)}{2K(n)};$$
$$n = \frac{L_g}{L_g + \Delta L_g}; \qquad m^2 + n^2 = 1 \tag{8}$$

and K is the complete elliptic integral of the first kind. The source resistance R_{ss} was determined by using the expressions shown at the bottom of the page [4]:

III. Simulation Results

Using the algorithm presented above, we have studied the dependences of the transverse delays on the GaAs/AlGaAs MODFET fabrication parameters. The values of the model parameters ρ_{12}, R_{c1}, R_{c2}, r_{s1}, and r_{s2} used in the analysis were those extracted from the measurements of the resistances of gated and ungated MODFET structures of various lengths [4]: $\rho_{12} = 1.5 \times 10^{-5}$ $(\Omega \cdot \mathrm{cm}^2)$, $R_{c1} = 0.255$ $(\Omega \cdot \mathrm{mm})$, $R_{c2} = 1.2$ $(\Omega \cdot \mathrm{mm})$, $r_{s1} = 216$ Ω, $r_{s2} = 1,164$ Ω. The values of other circuit elements used in this analysis were: $R_{gg} = 2.0 \times \rho \times 10^4$ (Ω/m), $L_{gg} = 10^{-6}$ $(\mathrm{H/m})$, $G_o = 0.1G_m$ where ρ is the gate electrode material resistivity. All values are per unit length (per meter) of the width of the MODFET. The overshoot and ringing observed in the curves for $i(t)$ are due to speed sensitivity of the MODFETs and the finite step size used to find $i(t)$.

Fig. 2 shows the dependence of the rise time on the gate length in the range $0.01-1$ μm. For these results, the width of the MODFET was fixed at 100 μm and the gate metal was aluminum with $\rho = 3$ $\mu\Omega \cdot$ cm. This figure shows that, for gate lengths less than approximately 0.4 μm, the rise time decreases when the gate length increases while, for gate lengths greater than 0.4 μm, the rise time increases when gate length increases. This can be explained as due to the increases in the capacitances C_{gs} and C_{gd} and the decrease in the gate resistance R_{gg} when the gate length is increased. In other words, the gate resistance dominates the delays when the gate length is less than approximately 0.4 μm while the capacitances dominate the delays for gate length greater than nearly 0.4 μm. Fig. 3 shows the normalized short-circuited drain currents for gate widths of 100 and 500 μm and the dependence of the rise time on the width of the MODFET is shown in Fig. 4. The increase in the propagation delays is due to increase in the capacitances C_{gs}, C_{gd} and decrease in the resistance R_{gg} as the MODFET width is increased. Fig. 5 shows the normalized short-circuited drain currents for gate metal resistivities of 100 and 1000 $\mu\Omega \cdot$ cm. For these results, the gate length was 0.5 μm and the width of the MODFET was 100 μm. It shows that, as the resistivity is increased, the drain current rises more slowly toward its

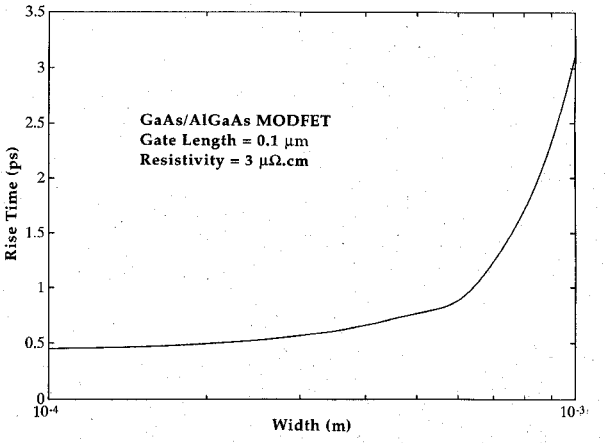

Fig. 4. Rise time in a typical GaAs/AlGaAs MODFET as a function of the width of the MODFET in the range $100-1000$ μm.

$$R_{ss} = \frac{r_{s1}r_{s2}L}{r_{s1}+r_{s2}} + \frac{\alpha_2 + \beta_2\cosh(K_1L) + \gamma_2 K_1\sinh(K_1L)}{(r_{s1}+r_{s2})^2\cosh(K_1L) + (r_{s1}+r_{s2})K_1(R_{c1}R_{c2})\sinh(K_1L)};$$
$$\alpha_2 = 2r_{s2}(r_{s1}R_{c2} - r_{s2}R_{c1}); \qquad \beta_2 = 2r_{s2}^2R_{c1} + \left(r_{s1}^2 + r_{s2}^2\right)R_{c2};$$
$$\gamma_2 = (r_{s1}+r_{s2})R_{c1}R_{c2} + r_s^2\rho_{12}; \qquad K_1 = \sqrt{\left(\frac{r_{s1}+r_{s2}}{\rho_{12}}\right)} \tag{9}$$

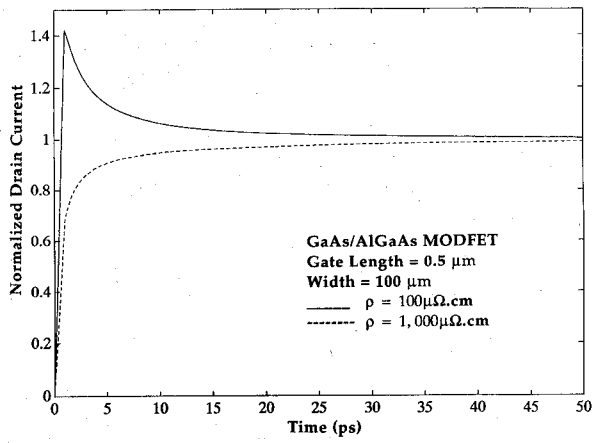

Fig. 5. Normalized short-circuited drain currents in a GaAs/AlGaAs MODFET for gate metal resistivities of 100 and 1000 $\mu\Omega \cdot$ cm in the range 0–50 ps.

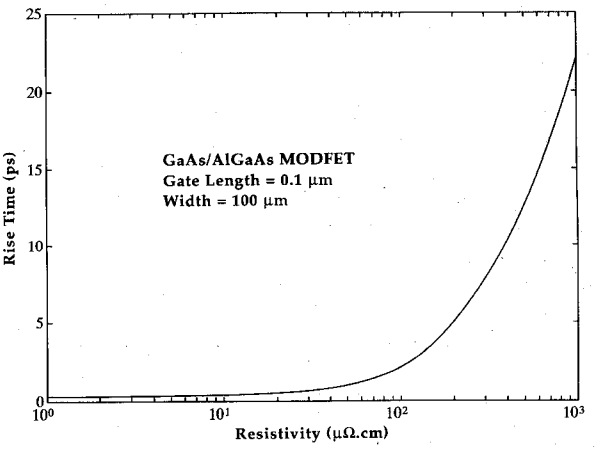

Fig. 6 Rise time in a typical GaAs/AlGaAs MODFET as a function of the gate metal resistivity in the range 1–1000 $\mu\Omega \cdot$ cm.

TABLE I
COMPARISON OF THE PROPAGATION DELAYS IN MESFETS AND MODFETS

FET Parameters	GaAs MESFET		GaAs/AlGaAs MODFET	
	Delay Time (ps)	Rise Time (ps)	Delay Time (ps)	Rise Time (ps)
Gate Length = 1.0 μm, Width = 100 μm, $\rho = 3\mu\Omega \cdot$cm	0.55	2.25	0.25	0.37
Gate Length = 0.5 μm, Width = 100 μm, $\rho = 3\mu\Omega \cdot$ cm	0.25	1.00	0.16	0.26
Gate Length = 0.5 μm, Width = 100 μm, $\rho = 100\ \mu\Omega \cdot$ cm	1.20	6.6	0.35	0.56

steady state value. This is further suggested by the dependence of the rise time on the gate metal resistivity shown in Fig. 6.

A comparison of the transverse delay times and rise times in a few GaAs MESFETs and GaAs/AlGaAs MODFETs with nearly the same common FET parameters is shown in Table I. The transverse delays in the GaAs MESFETs were determined by using the algorithm developed earlier [1] while those in the MODFETs were determined by using the algorithm presented in this paper. It shows that, as expected, the propagation delays in a MODFET are much smaller than in a MESFET with the same common technology parameters.

IV. CONCLUSIONS

The MODFET has been modeled as two lossy transmission lines coupled to each other by the gate-drain capacitances. The model is valid for MODFETs with submicron gate lengths and is suitable for inclusion in the CAD tools. Since Miller's theorem has been used to uncouple the gate and drain lines, the technique is valid for small signals and may fail for small gain. The simulation results can be utilized for optimization of the high-speed circuits.

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